

REMARKS/ARGUMENTS

Claims 1-29 were previously pending in the application. Claims 1-29 are canceled and new claims 30-58 are added herein. Assuming the entry of this amendment, claims 30-58 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

Support for new claims can be found in the specification, for example, as follows:

Claims 30, 41:	Figs. 3-4;
Claims 31, 32, 42, 53, 54:	page 9, line 18 through page 10, line 5; page 1, lines 18-20;
Claims 33, 43, 55:	page 10, lines 13-14;
Claims 34, 36, 37, 44, 46, 47:	Fig. 4;
Claims 35, 45:	Fig. 5;
Claims 38, 39, 48, 49:	page 12, lines 3-12;
Claims 40, 56:	page 10, line 15, through page 11, line 2;
Claims 50, 57:	Figs. 8-9; and
Claims 51, 52, 58:	Fig. 9.

In paragraph 1 of the office action, the Examiner objected to the drawings filed on December 13, 2001 for the indicated informalities. In response, the Applicant notes that a substitute set of drawings, which already corrected these informalities, was filed on March 6, 2002. The Applicant submits herewith a Transmittal of Corrected Drawings with a duplicate of the set of drawings filed on March 6, 2002.

In paragraph 3, the Examiner rejected claims 1-9, 16-17, and 28-29 under 35 U.S.C. § 102(e) as being anticipated by Bolla. In paragraph 5, the Examiner rejected claims 10-15 and 18-27 under 35 U.S.C. § 103(a) as being unpatentable over Bolla in view of admitted prior art (APA).

Since claims 1-29 are canceled, the rejections of those claims are now moot. For the following reasons, the Applicant submits that all pending claims are allowable over Bolla.

Claims 30-49:

Claim 30 is directed to an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network. The interface circuit has filter circuitry including a blocking capacitor (e.g., capacitor 28), which serves to separate signals between high- and low-frequency circuitry. High-frequency (e.g., ADSL) signals pass the blocking capacitor and are processed by the high-frequency circuitry while low-frequency (e.g., POTS) signals are substantially blocked from entering the high-frequency circuitry and are processed by the low-frequency circuitry. A subscriber line interface circuit (SLIC) and a coder/decoder (CODEC) located within the low-frequency circuitry serve, among other functions, to synthesize a desired impedance, e.g., that specified in the Telecordia Standard, between the tip and ring lines. However, the presence of the blocking capacitor, which is substantially connected in parallel to the SLIC, causes the effective impedance between the tip and ring lines to deviate from the desired impedance.

To mitigate this problem, the interface circuit incorporates a capacitor cancellation circuit (CCC, e.g., CCC 100 of Figs. 3 and 4) coupled across the blocking capacitor and adapted to generate a single-ended signal, which is applied to the SLIC and coupled via the SLIC and the filter circuitry to the tip/ring lines to cancel a portion of the effect of the blocking capacitor on the impedance of the tip/ring lines. In other words, the CCC reduces the deviation of the effective impedance between the tip and ring lines

from the desired impedance caused by the blocking capacitor, thereby partially offsetting the detrimental effect of that capacitor on the impedance.

Bolla discloses a circuit for interfacing between a pair of subscriber tip/ring lines and central office equipment of a network operator providing voice and DSL services. The circuit of Bolla has a POTS line card (e.g., card 105 of Fig. 1) and a DSL modem (e.g., modem 121 of Fig. 1), both coupled to the pair of subscriber tip/ring lines. The POTS line card has a SLIC and a CODEC adapted to synthesize a desired impedance between the tip and ring lines. The DSL modem incorporates a transformer (e.g., transformer 129 of Fig. 1) having a blocking capacitor (e.g., capacitor 141), which affects the effective impedance between the tip and ring lines. The circuit of Bolla mitigates this problem by incorporating into the POTS line card a negative impedance synthesis module (NISM, e.g., NISM 111 of Fig. 1). The NISM is coupled in parallel with the blocking capacitor and is adapted to synthesize a negative impedance, which compensates the impedance mismatch caused by the presence of the blocking capacitor (page 2, paragraph 0021).

Although the general effect of a NISM disclosed by Bolla (i.e., offsetting the detrimental influence of the blocking capacitor on the impedance) is similar to that of a CCC recited in claim 30, the NISM and the CCC operate based on different principles. More specifically, a NISM of Bolla is simply coupled across the blocking capacitor without forming any feedback loops with other circuit elements. For example, NISM 111 of Bolla is coupled across blocking capacitor 141 as shown in Bolla's Figs. 1, 2A, or 2B. In contrast, a CCC of claim 30 operates as a part of a feedback loop including several other circuit elements. For example, as shown in Fig. 3, CCC 100 is coupled across blocking capacitor 28 and generates a single-ended signal applied to port RCPV of SLIC 22. SLIC 22 is then coupled back to blocking capacitor 28 via filter 32 and the windings of transformer 26.

Claim 30 explicitly recites that the CCC is coupled across the blocking capacitor and adapted to generate a single-ended signal, which is applied to the SLIC and coupled via the SLIC and the filter circuitry to the tip/ring lines. The Applicant submits that Bolla does not teach or even suggest such a feature. Advantageously, an interface circuit recited in claim 30 can be implemented using only low-voltage components referenced to the same dc power supplies as the SLIC. As a result, such an interface circuit requires no additional floating power supplies and/or special lightning and fault protection. In addition, since the CCC is fully compatible with the SLIC circuitry, it can be integrated into the SLIC, thereby producing an interface circuit having a relatively low cost. In contrast, the NISM of Bolla does require several floating power supplies (see, e.g., Bolla's Fig. 4), which limits its compatibility with the SLIC and causes the corresponding interface circuit to be relatively expensive.

For all these reasons, the Applicant submits that claim 30 is allowable over Bolla. For similar reasons, the Applicant submits that claim 41 is also allowable over Bolla. Since claims 31-40 and 42-49 depend variously from claims 30 and 41, it is further submitted that those claims are also allowable over Bolla.

Claims 34 and 44 further specify that the CCC comprises (i) a first converter adapted to sense a differential voltage across the blocking capacitor and generate a single-ended capacitance signal that reflects the capacitance of the blocking capacitor; and (ii) a low-pass filter adapted to filter out components of the single-ended capacitance signal corresponding to the high-frequency signals to generate the single-ended signal applied to the SLIC. The Applicant submits that Bolla does not teach or suggest such a combination of features. This fact provides additional reasons for the allowability of claims 34 and 44, as well as claims 35-39 and 45-49, which depend variously from claims 34 and 44.

Claims 36 and 46 further specify that the first converter comprises an operational amplifier having two inputs coupled across the blocking capacitor and an output coupled to the low-pass filter. The Applicant submits that Bolla does not teach or suggest such a combination of features. This fact provides yet additional reasons for the allowability of claims 36 and 46, as well claims 37 and 47, which depend variously from claims 36 and 46.

Claims 37 and 47 further specify that the first converter comprises (i) a first capacitor and a first resistor coupled in series between a non-inverting input of the operational amplifier and a first terminal of the blocking capacitor; (ii) a second capacitor and a second resistor coupled in series between an inverting input of the operational amplifier and a first terminal of the blocking capacitor; (iii) a third capacitor and a third resistor coupled in parallel between the inverting input and the output of the operational amplifier; and (iv) a fourth capacitor and a fourth resistor coupled in parallel between the non-inverting input of the operational amplifier and the SLIC. The Applicant submits that Bolla does not teach or suggest such a combination of features. This fact provides yet additional reasons for the allowability of claims 37 and 47.

Claims 38-39 and 48-49 further specify that the low-pass filter is a fourth-order filter and that the low-pass filter comprises two serially connected second-order filters. The Applicant submits that Bolla does not teach or suggest such a combination of features. This fact provides yet additional reasons for the allowability of claims 38-39 and 48-49.

Claims 50-58:

Claim 50 is directed to an interface circuit for interfacing between a pair of subscriber tip/ring lines and a central office of a telecommunications network. The interface circuit has filter circuitry including a blocking capacitor (e.g., capacitor 28), which serves to separate signals between high- and low-frequency circuitry. High-frequency (e.g., ADSL) signals pass the blocking capacitor and are processed by the high-frequency circuitry while low-frequency (e.g., POTS) signals are substantially blocked from entering the high-frequency circuitry and are processed by the low-frequency circuitry. A subscriber line interface circuit (SLIC) and a coder/decoder (CODEC) located within the low-frequency circuitry serve, among other functions, to synthesize a desired impedance, e.g., that specified in the Telecordia Standard, between the tip and ring lines. However, the presence of the blocking capacitor, which is substantially connected in parallel to the SLIC, causes the effective impedance between the tip and ring lines to deviate from the desired impedance. To mitigate this problem, the interface circuit incorporates a capacitor cancellation circuit (e.g., CCC 162 of Figs. 8 and 9) coupled across the blocking capacitor and adapted to cancel a portion of the effect of the blocking capacitor on the impedance of the tip/ring lines. Claim 50 further specifies that the CCC includes:

- an operational amplifier having (i) an inverting input coupled to a first terminal of the blocking capacitor, (ii) a non-inverting input coupled to a second terminal of the blocking capacitor, and (iii) an output coupled back to the first and second terminals of the blocking capacitor; and

- an inverter coupled between the output of the operational amplifier and the first terminal of the blocking capacitor.

Bolla discloses a circuit for interfacing between a pair of subscriber tip/ring lines and central office equipment of a network operator. As already explained above, the circuit of Bolla has a negative impedance synthesis module (NISM) coupled across the blocking capacitor.

Although a NISM of Bolla and a CCC recited in claim 50 serve similar purposes (i.e., offsetting the detrimental influence of the blocking capacitor on the impedance), they have different circuit

structures. For example, Bolla teaches a NISM having two similarly configured operational amplifiers, one associated with the tip line and the other associated with ring line (see, e.g., page 5, paragraph 0038, and page 5, paragraph 0057). Representative examples of such operational amplifiers are (1) operational amplifiers **220a** and **220b** of Bolla's Fig. 2A, (2) operational amplifiers **270a** and **270b** of Bolla's Fig. 2B, and (1) operational amplifiers **415a** and **415b** of Bolla's Fig. 4. In contrast, claim 50 explicitly recites that the CCC has an operational amplifier (e.g., amplifier **164** of Fig. 9) and an inverter (e.g., inverter **166** of Fig. 9) coupled between the output of the operational amplifier and a terminal of the blocking capacitor. The operational amplifier and the inverter recited in claim 50 are not similarly associated with the tip/ring lines because, for example, the inputs of the operational amplifier are coupled to two terminals of the blocking capacitor, while the inverter is coupled between the output of the operational amplifier and one terminal of the blocking capacitor. The Applicant submits therefore that Bolla does not teach or even suggest a structure for his NISM having a combination of features recited in claim 50.

Advantageously, similar to the interface circuit of claim 30, an interface circuit recited in claim 50 can be implemented using only low-voltage components referenced to the same dc power supplies as the SLIC. As a result, such an interface circuit requires no additional floating power supplies and/or special lightning and fault protection. In addition, since the CCC is fully compatible with the SLIC circuitry, it can be integrated into the SLIC, thereby producing an interface circuit having a relatively low cost. In contrast, the NISM of Bolla does require several floating power supplies (see, e.g., Bolla's Fig. 4), which limits its compatibility with the SLIC and causes the corresponding interface circuit to be relatively expensive.

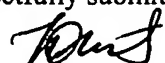
For all these reasons, the Applicant submits that claim 50 is allowable over Bolla. For similar reasons, the Applicant submits that claim 57 is also allowable over Bolla. Since claims 51-56 and 58 depend variously from claims 50 and 57, it is further submitted that those claims are also allowable over Bolla.

Claims 51 and 58 further specify that the CCC comprises (i) a first capacitor and a first resistor coupled in series between the inverting input of the operational amplifier and the first terminal of the blocking capacitor; (ii) a second capacitor and a second resistor coupled in series between the non-inverting input of the operational amplifier and the second terminal of the blocking capacitor; (iii) a third capacitor and a third resistor coupled in parallel between the inverting input and the output of the operational amplifier; and (iv) a fourth capacitor and a fourth resistor coupled in parallel between the non-inverting input of the operational amplifier and a ground terminal. The Applicant submits that Bolla does not teach or suggest such a combination of features. This fact provides additional reasons for the allowability of claims 51 and 57, as well as claim 52, which depends from claim 51.

In view of the above amendments and remarks, the Applicant believes that the now pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

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